IN THE CLAIMS:

Please amend the claims as set forth herein:

1. (Currently Amended) A method for fabricating a semiconductor memory device, comprising the steps of:

depositing first and second insulating layers on a semiconductor substrate having a ~~predetermined~~ shallow trench isolation (STI) region and a ~~predetermined~~ deep trench isolation (DTI) region;

forming the STI region by selectively etching the second and first insulating layers and the semiconductor substrate;

forming a photoresist to cover the STI region and expose the ~~predetermined~~ DTI region;

curing a surface of the photoresist by implanting high energy argon ions or through an e-beam process, ~~causing polymers in said photoresist to crosslink and thereby increasing an etch resistance of said photoresist~~ wherein implanting concentration of argon ions is $10^{12\sim15}$ cm^3 and implanting energy of argon ions is 10~200KeV, said argon employed only to supply energy to said photoresist; and

forming the DTI region by using only the cured photoresist and the second insulating layer as a mask.

Claims 2-3. (Canceled).

4. (Previously Presented) The method according to claim 1, wherein the curing step of the photoresist surface is performed by an e-beam curing process in which high energy electrons are passed through the surface of the photoresist.

5. (Previously Presented) The method according to claim 4, wherein an energy of the e-beam curing process is $1000 \sim 2000 uC/cm^2$.

6. (Previously Presented) The method according to claim 1, wherein the photoresist formation process includes an exposure process, which selects one light source among i-ray (365nm), KrF (248nm) and ArF(193nm).

7. (Original) The method according to claim 1, wherein the first insulating layer is a pad oxide layer.

8. (Original) The method according to claim 1, wherein the second insulating layer is a pad nitride layer.

9. (Currently Amended) The method according to claim 1, wherein the STI region has a depth of $2500 \sim 3000$Å from ~~the~~ a surface of the semiconductor substrate.

10. (Currently Amended) The method according to claim 1, wherein the DTI region has a depth of 7000 ~ 8000Å from ~~the~~ a surface of the semiconductor substrate.